EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20	714/14.ccls. and @pd>="20070511"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:03
L3	5	714/21.ccls. and @pd>="20070511"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:03
L4	14	714/22.ccls. and @pd>="20070511"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:05
L5	56	714/48.ccls. and @pd>="20070511"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:05
L6	286	(CPU or processor or "processing unit" or microprocessor) with (power or voltage or current) with (compatibility)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 15:02
L7	152	(CPU or processor or "processing unit" or microprocessor) with (power or voltage or current) with (compatibility) and (error or fault or failure)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:55
L8	2	(CPU or processor or "processing unit" or microprocessor) with (power or voltage or current) with (compatibility) and ((error or fault or failure) adj handler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:16
L9	454	(CPU or processor or "processing unit" or microprocessor) with (power) with (compat$7) and (error or fault or failure)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:56
L10	95	((CPU or processor or "processing unit" or microprocessor) with (power) with (compat$7)) and (handler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 13:56

EAST Search History

S1	17	(BROYLES-P BROYLES-PAUL BROYLES-PAUL-J BROYLES-PAUL-JAMES BROYLES-PAUL-JAMES-III BROYLES-PAUL-J-III).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 15:44
S2	6	("6718474" "6308240" "6365859"). pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/15 15:53
S3	986	714/48.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 09:11
S4	394	714/48.ccls. and power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 10:17
S5	89	714/48.ccls. and power and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 11:19
S6	59	714/48.ccls. and voltage and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 10:17
S7	267	714/14.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 13:01
S8	306	714/22.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 12:39
S9	81	714/21.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 13:16
S10	6	714/21.ccls. and power and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 10:16

EAST Search History

S11	5	714/21.ccls. and voltage and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 10:17
S12	41	714/21.ccls. and power	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 10:17
S13	813605	power and temperature	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 12:21
S14	464	"maximum power value"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 11:40
S15	5	"maximum power value" and "maximum temperature value"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 11:40
S16	10561	(power with (error failure fault)) and (temperature with (error failure fault))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 12:22
S17	5921	(power with (error failure fault)) with (temperature with (error failure fault))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 15:03
S18	642	(power with (error failure fault)) with (temperature with (error failure fault)) and "computer system"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 12:23
S19	0	(power with (error failure fault)) with (temperature with (error failure fault)) and "computer system" and ((error failure fault) adj handler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 12:23
S20	20	(power with (error failure fault)) with (temperature with (error failure fault)) and ((error failure fault) adj handler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/09/16 12:23

EAST Search History

S21	90	714/48.ccls. and @pd>="20060916"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 14:58
S22	21	714/22.ccls. and @pd>="20060916"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 12:39
S23	19	714/14.ccls. and @pd>="20060916"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/10/12 12:59
S24	11	714/21.ccls. and @pd>="20060916"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/11 13:16

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L16	216	714/48.ccls.	US-PGPUB	OR	ON	2007/10/12 15:01
L17	50	714/14.ccls.	US-PGPUB	OR	ON	2007/10/12 15:01
L18	72	(CPU or processor or "processing unit" or microprocessor) with (power or voltage or current) with (compatibility)	US-PGPUB	OR	ON	2007/10/12 15:02
L19	1922	(power with (error failure fault)) with (temperature with (error failure fault))	US-PGPUB	OR	ON	2007/10/12 15:03
L20	124	(power with (error failure fault)) with (temperature with (error failure fault)) and (register with (cpu or processor))	US-PGPUB	OR	ON	2007/10/12 15:04

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Central **processing unit** - Wikipedia, the free encyclopedia
Die of an Intel 80486DX2 **microprocessor** (actual size: 12×6.75 mm) in its packaging. Central **Processing Unit** (**CPU**), or sometimes simply **processor**, ...
en.wikipedia.org/wiki/Central_processing_unit - 107k - Cached - Similar pages

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The analyzer has a central **processing unit** including a **microprocessor** which .... This enables simultaneous monitoring of **voltage** and **current** in four analog ...
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Electrical parameter analyzer - US Patent 5574654
This enables simultaneous monitoring of **voltage** and **current** in four analog .... on boot ROM 202 boots **microprocessor** 212 and passes control to **CPU** 50. ...
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Microprocessor having **power** management circuitry with coprocessor support - US Patent 5632037 from Patent Storm. A **processing unit** includes a plurality of ...
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Terms used: CPU or processor or processing unit or microprocessor AND power or voltage or current AND compatibility

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1 A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance

Qiang Wu, Margaret Martonosi, Douglas W. Clark, V. J. Reddi, Dan Connors, Youfeng Wu, Jin Lee, David Brooks

November 2005 **Proceedings of the 38th annual IEEE/ACM International Symposium on Microarchitecture MICRO 38**

Publisher: IEEE Computer Society

Full text available: pdf(517.60 KB) Publisher Site

Additional Information: full citation, abstract, citings, index terms

Dynamic voltage and frequency scaling (DVFS) is an effective technique for controlling microprocessor energy and performance. Existing DVFS techniques are primarily based on hardware, OS timeinterrupts, or static-compiler techniques. However, substantially greater gains can be realized when control opportunities are also explored in a dynamic compilation environment. There are several advantages to deploying DVFS and managing energy/performance tradeoffs through the use of a dynamic compiler. Mo ...

2 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(385.22 KB)

Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

3 Networked sensor platforms: XYZ: a motion-enabled, power aware sensor node platform for distributed sensor network applications

Dimitrios Lymberopoulos, Andreas Savvides

April 2005 **Proceedings of the 4th international symposium on Information processing in sensor networks IPSN '05**

Publisher: IEEE Press
Full text available: pdf(188.45 KB) Additional Information: full citation, abstract, references, citings

This paper describes the XYZ, a new open-source sensing platform specifically designed to support our experimental research in mobile sensor networks. The XYZ node is designed around the OKI ML67Q500x ARM THUMB Microprocessor and the IEEE 802.15.4 compliant CC2420 radio from Chipcon. Its new features include support for two different CPU sleep modes and a long-term ultra low power sleep mode for the entire node. This allows the XYZ and its peripheral boards to transition into deep sleep for exte ...

4 Pen computing: a technology overview and a vision

André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3
Publisher: ACM Press
Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

5 Signal and power delivery integrity: Optimal selection of voltage regulator modules in a power delivery network

Behnam Amelifard, Massoud Pedram
June 2007 **Proceedings of the 44th annual conference on Design automation DAC '07**
Publisher: ACM Press
Full text available: pdf(368.34 KB) Additional Information: full citation, abstract, references, index terms

High efficiency low voltage DC-DC conversion is a key enabler to the design of power-efficient integrated circuits. Typically a star configuration of the DC-DC converters, where only one converter resides between the source and each load, is used to deliver currents with appropriate voltage levels to different loads in the circuit. In this paper we show that using a tree topology of suitably chosen voltage regulators between the power source and loads yields higher power efficiency in the pow ...

Keywords: DC-DC converter, low-power design, power delivery network, voltage regulator

6 VLIW instruction scheduling for minimal power variation

Shu Xiao, Edmund M.-K. Lai
September 2007 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 4 Issue 3
Publisher: ACM Press
Full text available: pdf(796.99 KB) Additional Information: full citation, abstract, references, index terms

The focus of this paper is on the minimization of the variation in power consumed by a VLIW processor during the execution of a target program through instruction scheduling. The problem is formulated as a mixed-integer program (MIP) and a problem-specific branch-and-bound algorithm has been developed to solve it more efficiently than generic MIP solvers. Simulation results based on the TMS320C6711 VLIW digital signal processor using benchmarks from Mediabench and Trimaran showed that over 40 ...

Keywords: Instruction scheduling, VLIW processors, power variation reduction

7 Design issues for dynamic voltage scaling

Thomas D. Burd, Robert W. Brodersen

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design ISLPED '00**

Publisher: ACM Press

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references, citings, index terms

Processors in portable electronic devices generally have a computational load which has time-varying performance requirements. Dynamic Voltage Scaling is a method to vary the processors supply voltage so that it consumes the minimal amount of energy by operating at the minimum performance level required by the active software processes. A dynamically varying supply voltage has implications on the processor circuit design and design flow, but with some minimal constraints it is straightforwa ...

Keywords: circuit design, energy efficient, processor, variable voltage

8 Energy aware design: Dynamic frequency and voltage control for a multiple clock domain microarchitecture

Greg Semeraro, David H. Albonesi, Steven G. Dropsho, Grigorios Magklis, Sandhya Dwarkadas, Michael L. Scott

November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture MICRO 35**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.17 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe the design, analysis, and performance of an on--line algorithm to dynamically control the frequency/voltage of a Multiple Clock Domain (MCD) microarchitecture. The MCD microarchitecture allows the frequency/voltage of microprocessor regions to be adjusted independently and dynamically, allowing energy savings when the frequency of some regions can be reduced without significantly impacting performance.Our algorithm achieves on average a 19.0% reduction in Energy Per Instruction (EPI) ...

9 Energy Optimization of Distributed Embedded Processors by Combined Data Compression and Functional Partitioning

Jinfeng Liu, Pai H. Chou

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design ICCAD '03**

Publisher: IEEE Computer Society

Full text available: pdf(271.86 KB) Additional Information: full citation, abstract, citings, index terms

Transmitting compressed data can reduce inter-processor communicationtraffic and create new opportunities for DVS (dynamicvoltage scaling) in distributed embedded systems. However, datacompression alone may not be effective unless coordinated withfunctional partitioning. This paper presents a dynamic programmingtechnique that combines compression and functional partitioningto minimize energy on multiple voltage-scalable processorsrunning pipelined data-regular applications under performance cons ...

10 Processor frequency setting for energy minimization of streaming multimedia application

Andrea Acquaviva, Luca Benini, Bruno Riccò

April 2001 **Proceedings of the ninth international symposium on Hardware/software**

codesign CODES '01
Publisher: ACM Press
Full text available: pdf(401.70 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we describe a software-controlled approach for adaptively minimizing energy in embedded systems for realtime multimedia processing. Energy is optimized by clock speed setting: the software controller dynamically adjusts processor clock speed to the frame rate requirements of the incoming multimedia stream. The speed-setting policy is based on a system model that correlates clock speed with best-case, average-case and worst-case sustainable frame rate, accounting for data-depend ...

11 Architecture of the IBM system/370
Richard P. Case, Andris Padegs
January 1978 **Communications of the ACM**, Volume 21 Issue 1
Publisher: ACM Press
Full text available: pdf(2.78 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses the design considerations for the architectural extensions that distinguish System/370 from System/360. It comments on some experiences with the original objectives for System/360 and on the efforts to achieve them; and it describes the reasons and objectives for extending the architecture. It covers virtual storage, program control, data-manipulation instructions, timing facilities, multiprocessing, debugging and monitoring, error handling, and input/output operations. ...

Keywords: architecture, computer systems, error handling, instruction sets, virtual storage

12 SPOTS'06 session 4--new sensors and architectures: The low power energy aware processing (LEAP)embedded networked sensor system
Dustin McIntire, Kei Ho, Bernie Yip, Amarjeet Singh, Winston Wu, William J. Kaiser
April 2006 **Proceedings of the fifth international conference on Information processing in sensor networks IPSN '06**
Publisher: ACM Press
Full text available: pdf(200.80 KB) Additional Information: full citation, abstract, references, cited by, index terms

A broad range of embedded networked sensor (ENS) systems for critical environmental monitoring applications now require complex, high peak power dissipating sensor devices, as well as on-demand high performance computing and high bandwidth communication. Embedded computing demands for these new platforms include support for computationally intensive image and signal processing as well as optimization and statistical computing. To meet these new requirements while maintaining critical support for ...

Keywords: embedded wireless networked sensor, energy-aware multiprocessor platform, sensor platform hardware and software architecture

13 Low power implementation of a turbo-decoder on programmable architectures
Frank Gilbert, Alexander Worm, Norbert Wehn
January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**
Publisher: ACM Press
Full text available: pdf(109.44 KB) Additional Information: full citation, abstract, references, citings, index terms

Low Power is an extremely important issue for future mobile radio systems. Channel decoders are essential building blocks of base-band signal processing units in mobile terminal architectures. Thus low power implementations of advanced channel decoding techniques are mandatory. In this paper we present a low power implementation of the most sophisticated channel decoding algorithm (Turbo-decoding) on programmable architectures. Low power optimization is performed on two abstraction levels: ...

14 Pruning-based, energy-optimal, deterministic I/O device scheduling for hard real-time systems

Vishnu Swaminathan, Krishnendu Chakrabarty
February 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4 Issue 1
Publisher: ACM Press

Full text available: pdf(468.15 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Software-controlled (or dynamic) power management (DPM) in embedded systems has emerged as an attractive alternative to inflexible hardware solutions. However, DPM via I/O device scheduling for hard real-time systems has received relatively little attention. In this paper, we present an offline I/O device scheduling algorithm called energy-optimal device scheduler (EDS). For a given set of jobs, it determines the start time of each job such that the energy consumption of the I/O devices is minim ...

Keywords: I/O devices, Schedulability analysis, device scheduling, hard real-time systems

15 Embedded systems: A VLIW low power Java processor for embedded applications

Antonio Carlos S. Beck, Luigi Carro
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design SBCCI '04**
Publisher: ACM Press

Full text available: pdf(303.80 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a pioneer VLIW architecture of a native Java processor. We show that, thanks to the specific stack architecture and to the use of the VLIW technique, one is able to obtain a meaningful reduction of power dissipation, with small area overhead, when compared to other ways of executing Java in hardware. The underlying technique is based on the reuse of memory access instructions, hence reducing power during memory or cache accesses. The architecture is validated for some complex ...

Keywords: Java, VLIW, power consumption

16 Power reduction techniques for microprocessor systems

Vasanth Venkatachalam, Michael Franz
September 2005 **ACM Computing Surveys (CSUR)**, Volume 37 Issue 3
Publisher: ACM Press

Full text available: pdf(602.33 KB) Additional Information: full citation, abstract, references, index terms

Power consumption is a major factor that limits the performance of computers. We survey the "state of the art" in techniques that reduce the total power consumed by a microprocessor system over time. These techniques are applied at various levels ranging from circuits to architectures, architectures to system software, and system software to applications. They also include holistic approaches that will become more important over the next decade. We conclude that power management is a ...

Keywords: Energy dissipation, power reduction

17 Architectures: A flexible simulation framework for graphics architectures

J. W. Sheaffer, D. Luebke, K. Skadron

August 2004 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware HWWS '04**

Publisher: ACM Press

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we describe a multipurpose tool for analysis of the performance characteristics of computer graphics hardware and software. We are developing Qsilver, a highly configurable micro-architectural simulator of the GPU that uses the Chromium system's ability to intercept and redirect an OpenGL stream. The simulator produces an annotated trace of graphics commands using Chromium, then runs the trace through a cycle-timer model to evaluate time-dependent behaviors of the varios functional ...

18 Energy-aware design of embedded memories: A survey of technologies, architectures, and optimization techniques

Luca Benini, Alberto Macii, Massimo Poncino

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Publisher: ACM Press

Full text available: pdf(288.44 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded systems are often designed under stringent energy consumption budgets, to limit heat generation and battery size. Since memory systems consume a significant amount of energy to store and to forward data, it is then imperative to balance power consumption and performance in memory system design. Contemporary system design focuses on the trade-off between performance and energy consumption in processing and storage units, as well as in their interconnections. Although memory design is as ...

Keywords: Embedded systems, embedded memories, integration, memories, nonvolatile, system-on-a-chip, volatile

19 The energy complexity of register files

V. Zyuban, P. Kogge

August 1998 **Proceedings of the 1998 international symposium on Low power electronics and design ISLPED '98**

Publisher: ACM Press

Full text available: pdf(923.77 KB) Additional Information: full citation, abstract, references, citings, index terms

Register files (RF) represent a substantial portion of the energy budget in modern processors, and are growing rapidly with the trend towards wider instruction issue. The actual access energy costs depend greatly on the register file circuitry used. This paper compares various RF circuitry techniques for their energy ef- ficiencies, as a function of architectural parameters such as the number of registers and the number of ports. The Port Priority Selection technique was found to be the ...

20 Regular contributions: DSP architectures: past, present and futures

Edwin J. Tan, Wendi B. Heinzelman

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Publisher: ACM Press
Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references

As far as the future of communication is concerned, we have seen that there is great demand for audio and video data to complement text. Digital signal processing (DSP) is the science that enables traditionally analog audio and video signals to be processed digitally for transmission, storage, reproduction and manipulation. In this paper, we will explain the various DSP architectures and its silicon implementation. We will also discuss the state-of-the art and examine the issues pertaining to pe ...

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